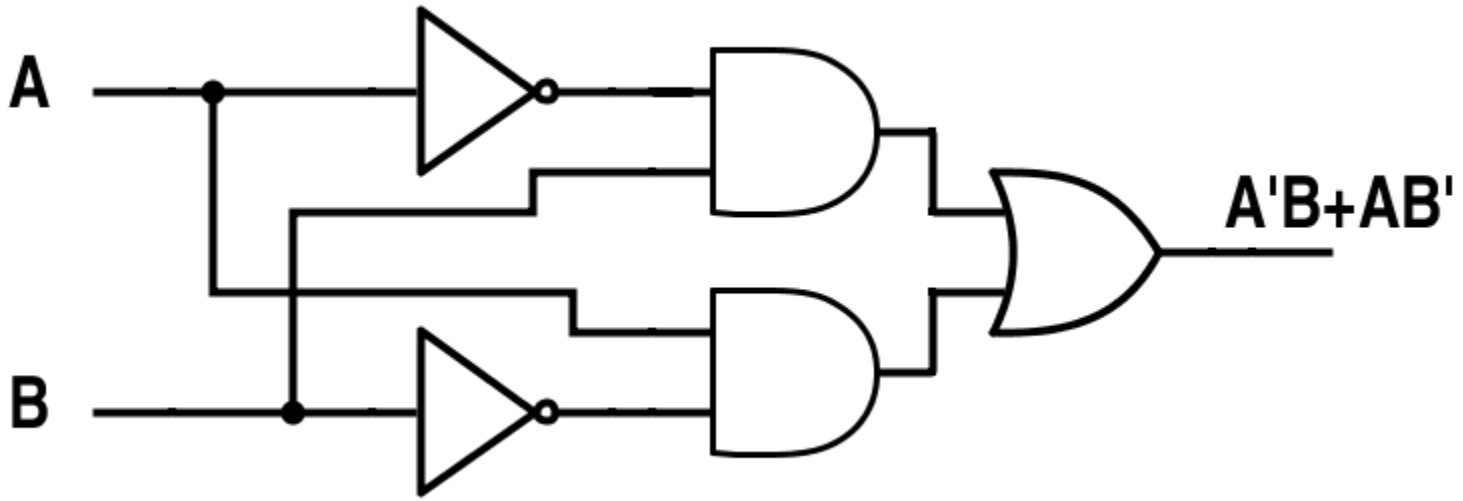
VHDL과 CPLD를 사용한 조합논리회로 설계

Combinational Logic Circuit (조합논리회로)

$$F = A' \cdot B + A \cdot B'$$

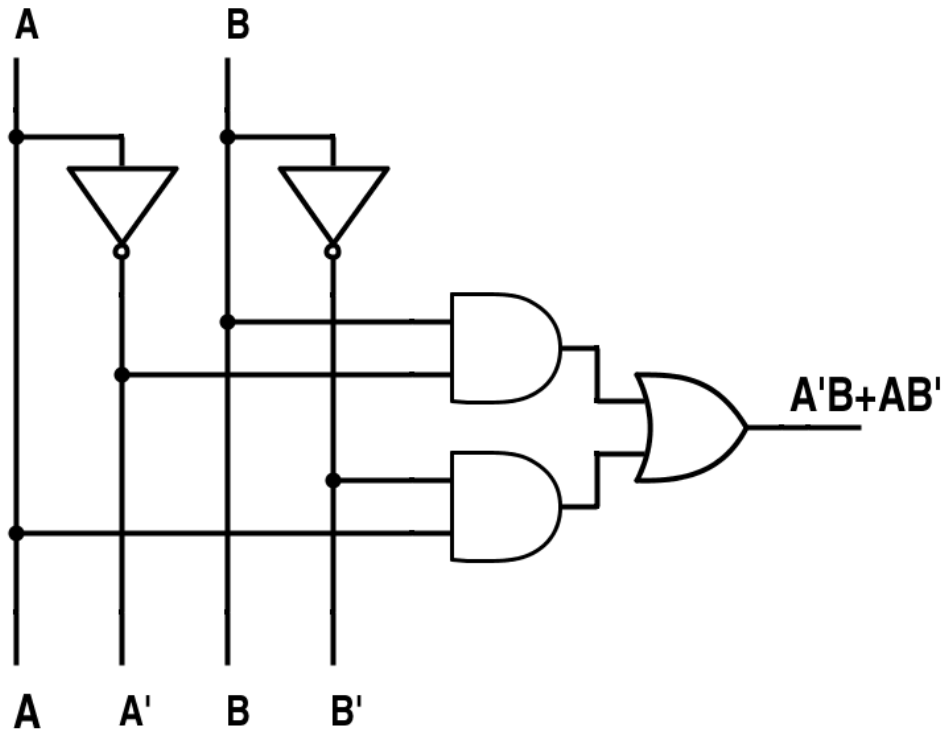
Implementation using gates



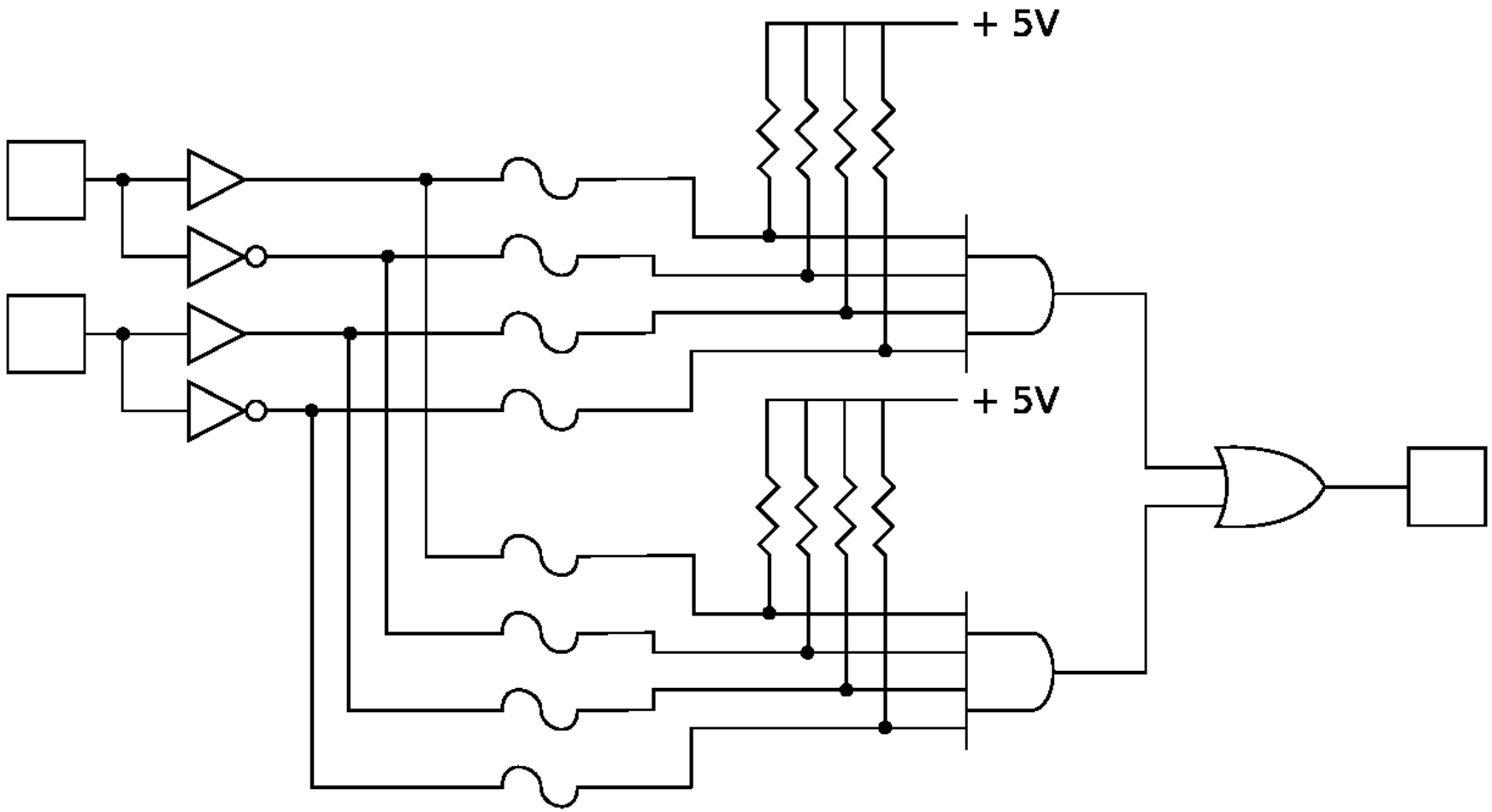
Combinational Logic Circuit (조합논리회로)

$F = A' \cdot B + A \cdot B'$

Implementation using gates

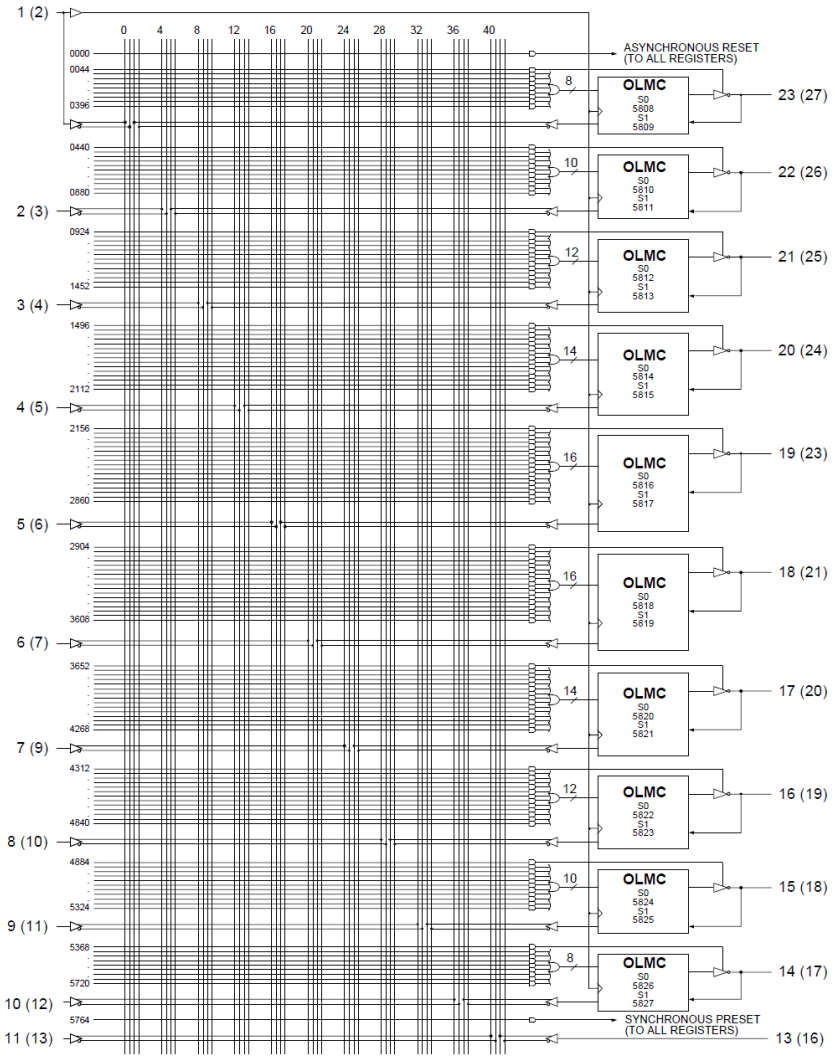


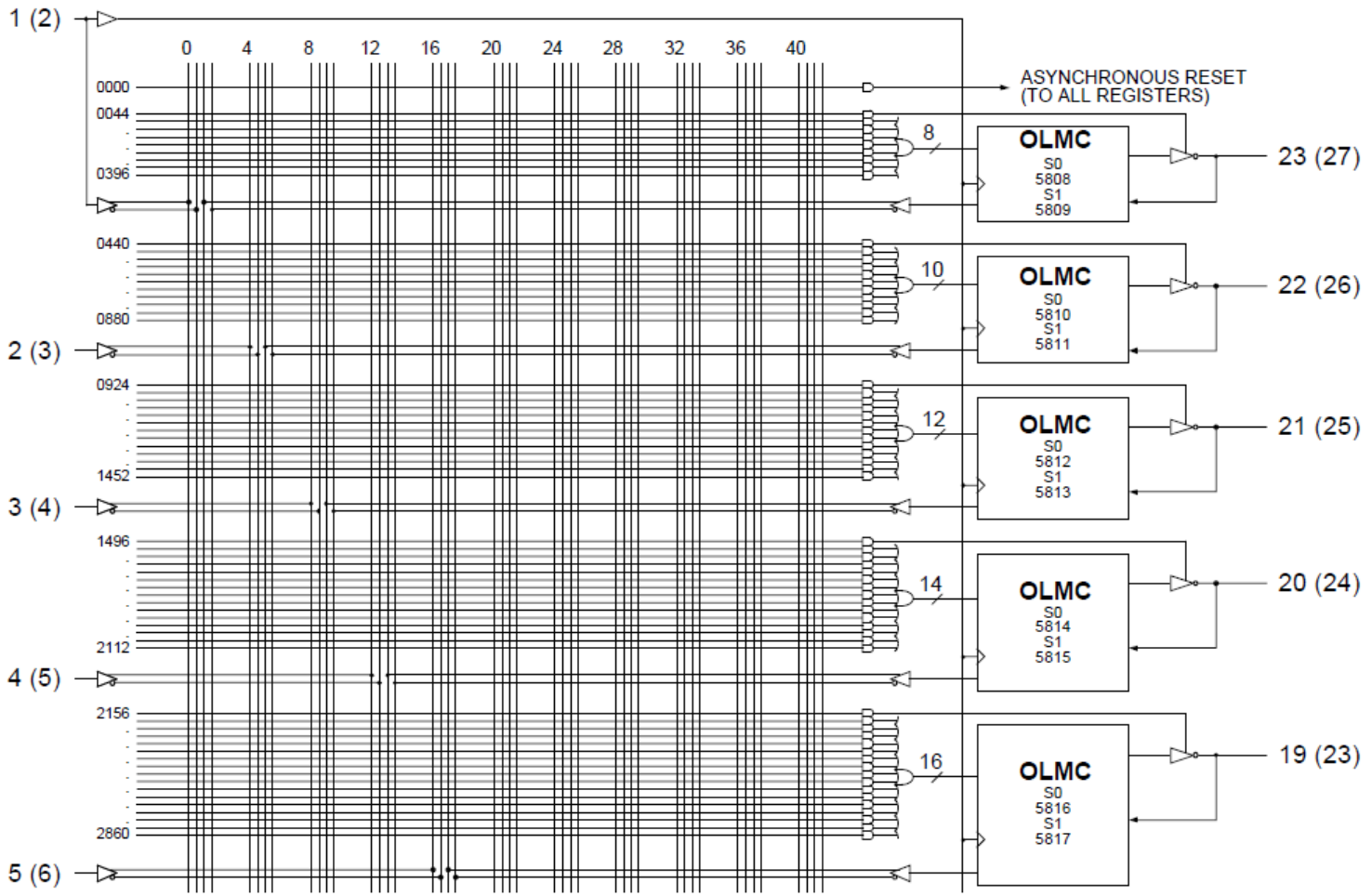
Programmable Logic Device (PLD)



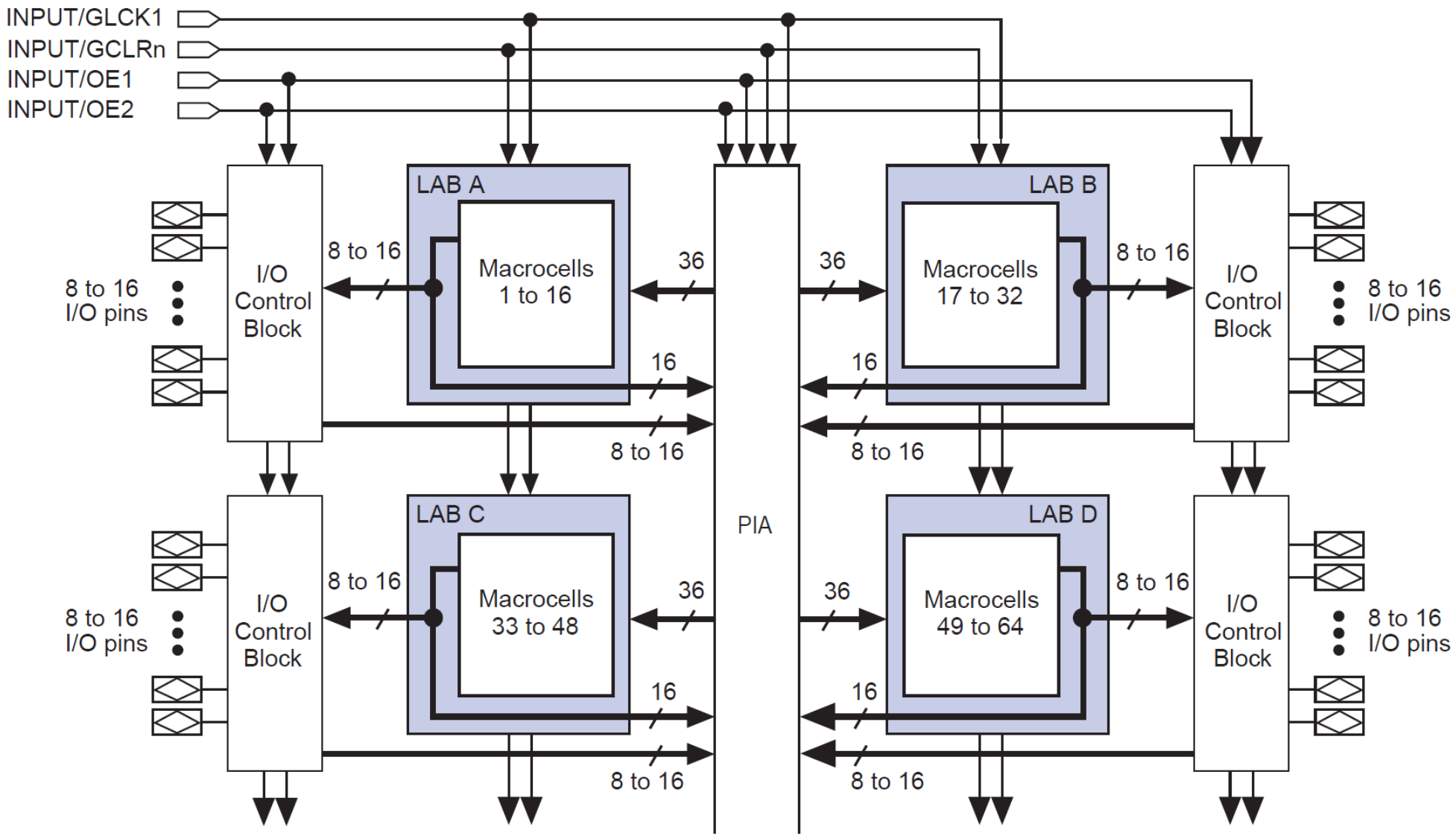
Simplified programmable logic device

Programmable Logic Device (PLD)

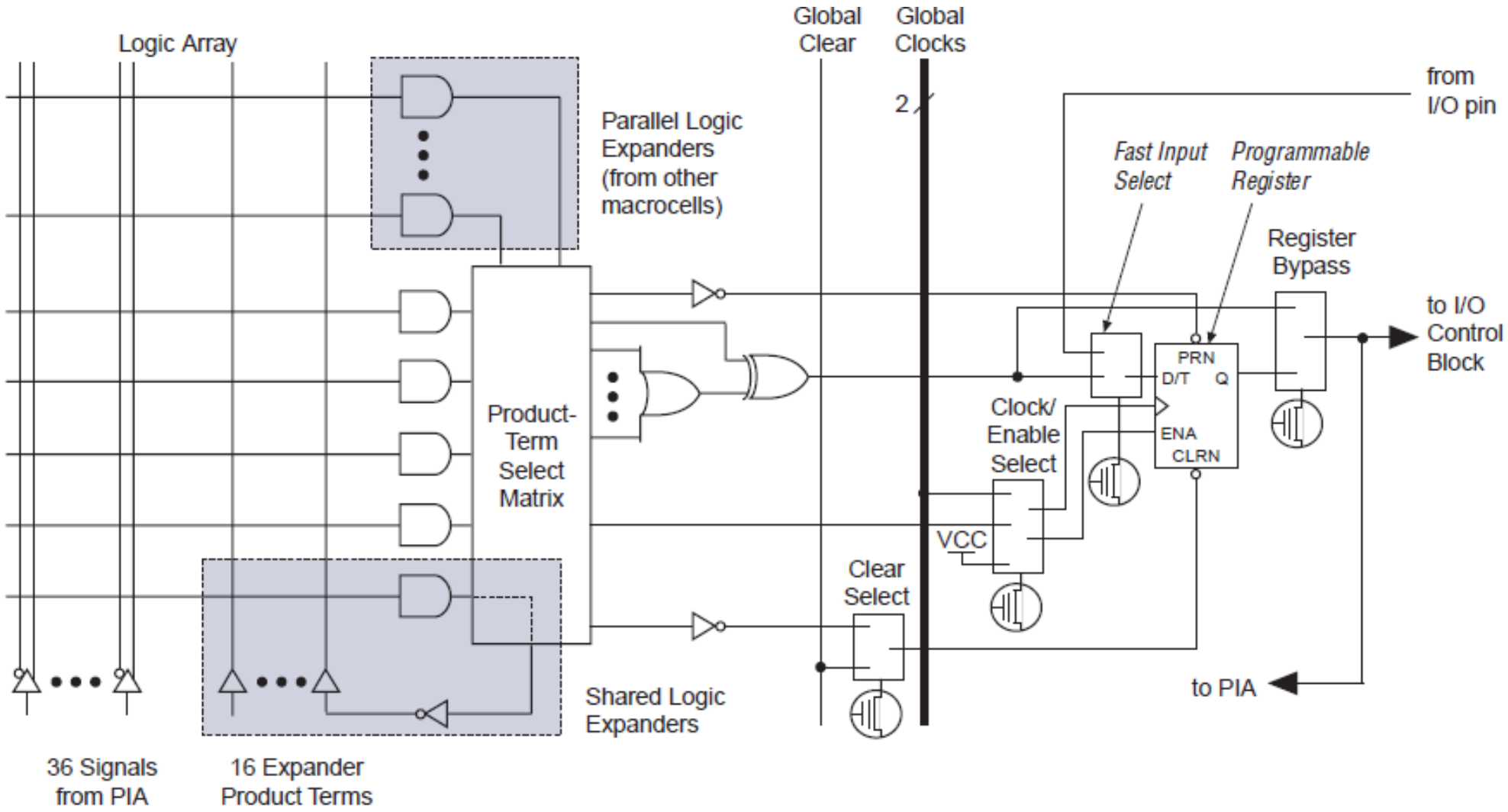




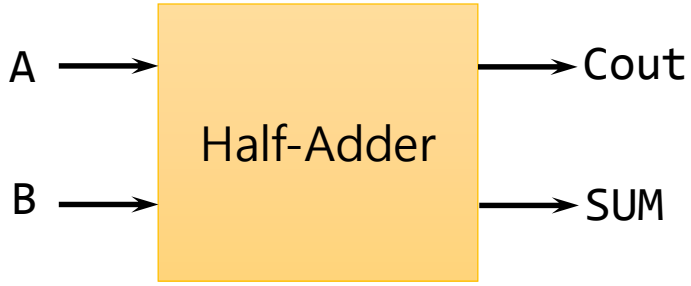
Complex Programmable Logic Device (CPLD)



Complex Programmable Logic Device (CPLD)

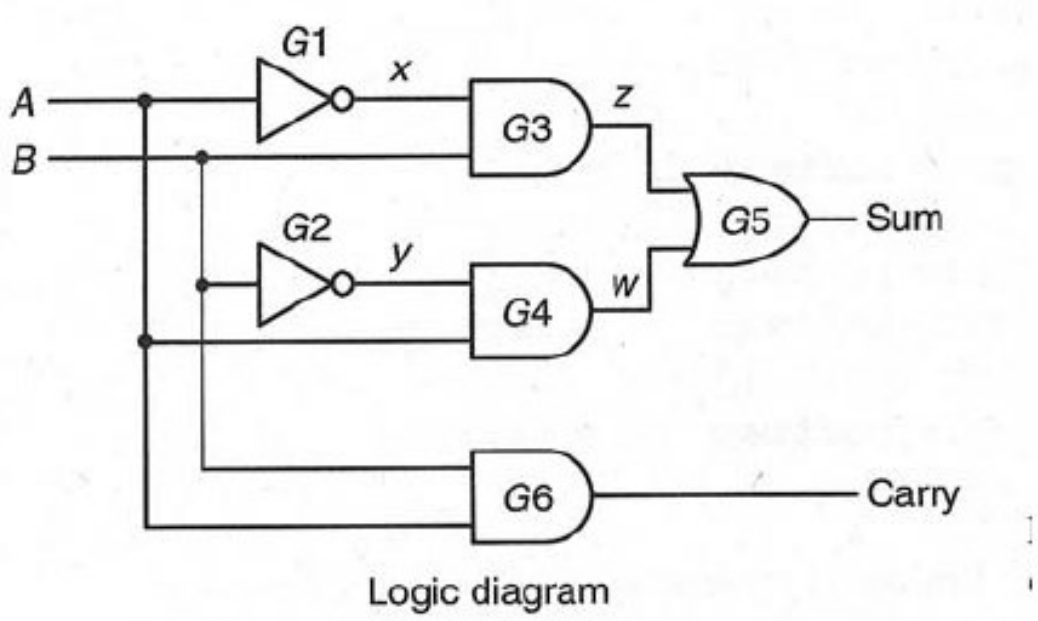


Half-Adder using Basic Gates



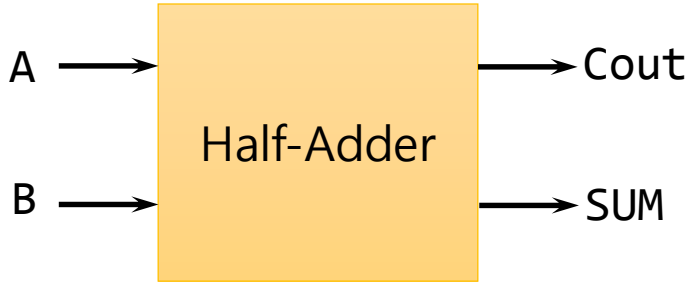
$$SUM = A \oplus B$$
$$Cout = A \cdot B$$

A	B	Cout	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Logic diagram

VHDL Code for Half-Adder



A	B	Cout	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$SUM = A \oplus B$$
$$Cout = A \cdot B$$

```
-- this is a VHDL comment
-- import std_logic from the IEEE library

library IEEE;
use IEEE.std_logic_1164.all;

-- this is the entity
entity HALF_ADDER is
    port (  A: in  std_logic;
            B: in  std_logic;
          SUM: out std_logic;
         COUT: out std_logic);
end entity HALF_ADDER;

-- this is the architecture
architecture MY_HALF_ADDER of HALF_ADDER is
    begin
        SUM  <= A xor B;
        COUT <= A and B;
    end architecture MY_HALF_ADDER;

-- end of file
```